A Literature Survey of FPGA Implementation of Inverter Techniques

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ABSTRACT- This paper reviews state of the art of multilevel inverter topologies using FPGA technology. Power electronics tools are which changes DC power to AC power at needed output voltage and frequency stage is known as inverters. Multilevel inverter has three dissimilar main topologies have been useful in industrial functions: Cascaded H-bridges converter, Diode clamped, and Flying capacitor multilevel inverter. This paper presents a review on various types of multilevel inverter (MLI) FPGA implementation. For the implementation of MLI using two type of phenomena in VHDL, the first one is CPLD and the second one is FPGA. FPGA is more popular as compare to CPLD now a day. In this survey paper give the brief over view of multi-level inverter (MLI) and different technique of MLI.

KEYWORDS— Multilevel inverter, PWM, FPGA, CPLD and VHDL

I. INTRODUCTION

Most PWM control systems implemented by analogy rely on "normal" sampled controlling strategies. More recently; a new switching strategy called "ordinary sampling" has been planned, which is considered to have a amount of benefits when implemented by digital techniques. Because natural and regular sampling methods can be implemented using microprocessor expertise, and are therefore likely to form the basis of most microprocessor PWM controls.

The core of any PWM control plan is undoubtedly the switching method used to generate the switching perimeters of the PWM control waveform. It is possible to study the literature over the past decade to track the historical evolution of PWM switching techniques and to link these developments to technology changes from analog systems through discrete digital control systems and more recently from Microprocessors. [1].

II. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

FPGAs are an efficient material for rapid prototyping. Its functions are quite complex to implement more of the glue logic. As the logical capacity of FPGAs increases, the synthesis of PGA becomes more and more important. One solution to designing large designs effectively is to use VHDL synthesis. Xilinx Field Programmable Gate Array (FPGA) is a user-programmable device. [1]

III. XILINX FPGA PWM GENERATOR

FPGA is a Programmable Logic Device developed by Xilinx, Inc. It includes thousands of logic gates. Some of them combine to form a configurable logic block (CLB). CLB simplifies the design of higher level circuits. Door interconnections using software are defined by SFL4M or ROM. This makes it possible to modify the designed circuit without modifying the hardware plate. Simultaneous operation, less hardware, easy and quick circuit modification

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comparatively low cost for a complex circuit and rapid prototyping make it the most favorable choice for prototyping an ASIC. [1]

III. LITERATURE REVIEW

A. S. Mekhilef, A. Masaoud, “Xilinx FPGA Based Multilevel PWM Single Phase Inverter”, 2006

Summary- In this paper, a single-phase PWM multi-level XILINX FPGA inverter was built by adding up bidirectional controls to the conventional link topology. The inverter can create three and five dissimilar output voltage points on the load. XILINX FPGA is a programmable logic device developed by XILINX which is considered an efficient material for rapid prototyping. It is used as a PWM generator to apply the appropriate signals to the inverter switches. In addition to XILINX FPGA, the Matlab / Simulink software was used for simulation and verification of the proposed circuit before implementation, simulation and experimental results show that the two are in close collaboration. The switching patterns adopted are applied to the six switches of the inverter to generate five or three levels of output voltage at different modulation indices. XILINX FPGA allows for easy, fast and flexible design and implementation. The experimental and simulated results give satisfactory results in terms of total harmonic distortion and shape of the current waveform and the output voltage. [2]


Summary- This paper presents a sinewave pulse width modulation (SPWM) controller based on a Programmable Carrier Module (FPGA) for ASD (High Speed Drive) applications powered by a single-phase, multi-level drive. The cascade inverter is built using three conventional H-bridges for a seven-level output that reduces harmonic content. The PWM Voltage Inverter (VSI) must maintain the voltage and frequency variation simultaneously and maintain their constant ratio for speed control. In this study, a simple SPWM control circuit is adopted using an FPGA device. It can be housed in a single chip that provides high computing speed and precise control signals for higher output voltages and currents with fewer harmonics. The VHDL language is used to model the switching strategies of the inverter. The proposed controller generates 12 control switching signals which in multi-level inverter cascade for 7 output voltage levels. The Matlab / System and ISE / XILINX tools are used with the hardware co-simulation to synthesize the digital control architecture and the architecture obtained I incorporated into FPGA. The sinusoidal PWM technique is adopted with FPGA to generate switching models. These switching pulses are applied to the multi-level inverter in cascade to generate an output voltage of 7 levels. This controller design is simulated and the compilation part is tested by FPGA in real time using hardware co-simulation. FPGA allows a simple, fast and flexible implementation of the controller circuit in the hardware. It can effectively adjust the modulation index range for variable speed control of the induction motor. The effective regulator maintains the constant voltage / frequency ratio. The simulation with experimental results demonstrates the quality of the voltage and current waveforms with less harmonic content at the output of the cascade inverter. These inverter topologies with digital control circuitry can be used for speed control of the induction motor and other medium scale industrial applications. [3]

C. Jagdish Kumar, Biswarup Das, Pramod Agarwal, “Harmonic reduction technique for a cascade multilevel inverter”, 2009

Summary- In this research, an optimization technique is proposed to calculate the switching angles at the fundamental frequency of the switching system by solving nonlinear transcendental equations (called selective harmonic elimination equations), thus eliminating certain harmonics predominant in And at the same time control the amplitude of the output voltage of a multi-level inverter is reached. Since these equations are of a non-linear transcendental nature, there may be a single, multiple or even a particular value of a modulation index. The proposed scheme is implemented so that all possible solutions are obtained without knowing the appropriate initial estimation solutions. Moreover, this technique is
suitable for the high level of multilevel inverters where other existing methods fail to calculate the switching angles due to a higher design load. For the modulation index values for which there are many solutions, the solutions that produce less THD in the output voltage are selected. A significant decrease in DHT is obtained by considering several sets of solutions instead of taking a single set of solutions. The results of the calculations are displayed graphically to better understand and prove the effectiveness of the method. An experimental 11-level multilevel cascade inverter is used to validate the results of the calculation. [4]

D. Jin Wang, Damoun Ahmadi, “A Precise and realistic Harmonic Elimination technique for Multilevel Inverters” 2010

Summary- Multi-level inverters have been widely used in medium and high voltage applications. Selective harmonic elimination for the voltage waveform generated by the staircase multi-level inverter has been extensively studied over the past decade. Most published methods on this subject were based on the resolution of multivariate groups of high-order polynomial equations from the expansion of the Fourier series. This research presents a different approach, based on criteria of equal and harmonic injection zone. With the proposed method, regardless of the number of voltage levels involved, only four simple equations are required. The results of a case study with up to five switching angles show that the proposed method can be used to achieve excellent harmonic removal performance of the modulation index range of at least 0.2 to 0.9. To demonstrate the adaptability of the method proposed for waveforms with a large number of switching angles, experimental results on a multi-level inverter of level 1-MVA 6000 V-17 are also presented at the end of this search. [5]

E. Swamit S. Tannu Dr. R. R. Sawant Dr. Y. S. Rao, “Discrete Time Control Technique for Induction Heating System”, 2012

Summary- A new discrete temporal control technique for the induction heating system is discussed. The system of discrete time control is modular and flexible compared to its continuous counterpart. This control system has major advantages of phase change control and pulse density modulation. The complete performance analysis of the newly developed algorithm was performed by conventional load simulations and hardware in loop simulation (HILS). Superior to the conventional control technique, this technique allows us to implement a configurable control system on an embedded processor. A complete discrete time control technique was developed for the induction heating system based on VS-SRI. The control technique has been validated by simulating different load scenarios. It is observed that the algorithm succeeded in regulating the power without losing ZVS over a wide range of load variations. It is possible to implement this algorithm in the embedded processor because the algorithm requires sampling rates that are commercially feasible even at very high resonance frequencies. [6]

F. M. Mythili, N. Kayalvizhi, “Harmonic Minimization in Multilevel Inverters Using Selective Harmonic Elimination PWM Technique” 2013

Summary- In general, the output voltage of the inverter must be sinusoidal. However, the waveforms of practical non-sinusoidal inverters and contain certain harmonics. For low and medium power applications, square or quasi-square waves may be acceptable, but for high power applications, weakly distorted sinusoidal waveforms are required. By number of levels in the inverter by increasing the output voltage has several steps generating a form of staircase, which reduces the harmonic distortion. Emerges need a multi-level inverter. In this cascading research work of the multi-level inverter with selective suppression of pulse width modulation harmonic (SHE-PWM) technique is implemented. The SHE-PWM problem is to solve the nonlinear transcendental equations that are used to determine the switching angles. Here, the evolutionary algorithm based on natural selection is proposed to solve the equations that reduce the computational load resulting from faster convergence. The main advantages are the reduction of the total
harmonic distortion and the low switching frequency. To validate the calculation results for the switching angles, a simulation is performed in the MATLAB / Simulink software tool for a level 7 Cascaded H bridge inverter. [7]

IV. RESULT PARAMETERS

In the FPGA implementation when discussing the result parameters. The result parameters are the total number of B1Os, the total number of Flip-flops, the total number of look-up tables, the total number of multipliers and the DSP slices. There are basic terms are used in FPGA technologies.

The flip-flops are binary shift registers used to synchronize logic and save logic states between clock cycles in an FPGA circuit. On each clock edge, a flip-flop locks the value 1 or 0 (TRUE or FALSE) on its input and holds this value constant until the next clock edge.

Much of the logic in a CLB is implemented using very small amounts of RAM in the form of LUTs. It is easy to assume that the number of system doors in an FPGA refers to the number of NAND gates and NOR gates in a particular chip. But in reality, any combinational logic (ANDs, ORs, NANDs, XORs, etc.) is implemented as truth tables in the LUT memory. A truth table is a predefined list of outputs for each combination of inputs.

Imagine now multiplying two 32-bit numbers together, and you end up with over 2000 operations for a single multiplication. For this reason, FPGAs have pre-built multiplier circuits to save on LUT and use flip-flops in mathematical applications and signal processing.

Many signal processing algorithms involve retaining the total number of multiplied numbers and therefore higher performance FPGAs such as Xilinx Virtex-5 FPGAs have pre-built multiplication and accumulation circuits. These pre-built processing blocks, also known as DSP48 slices, incorporate a 25-bit by 18-bit multiplier with an adder circuit.

Memory resources are another key specification to consider when selecting FPGAs. User-defined RAM, built into the entire FPGA chip, is useful for storing data sets or passing values between parallel tasks. Depending on the FPGA family, you can configure the built-in RAM in blocks of 16 or 36 kb. You still have the ability to implement datasets as arrays using flip-flops; However, large matrices quickly become costly for FPGA logical resources. A matrix of 100 elements of 32-bit numbers can consume more than 30 percent of the flip-flops in a Virtex-II 1000 FPGA or take less than 1 percent of the integrated block RAM. Digital signal processing algorithms often have to keep track of an entire block of data, or coefficients of a complex equation, and without embedded memory, many processing functions do not fit into the configurable logic of an FPGA chip.

The inherent parallel execution of FPGAs allows independent pieces of hardware logic to be driven by different clocks. Data transmission between logics operating at different speeds can be tricky, and on-board memory is often used to smooth transfer using FIFO (first-in first-out) memory buffers.

With this understanding of fundamental FPGA components, you can clearly see the advantage of implementing your logic in hardware circuits: you can achieve improvements in execution speed, reliability and flexibility. However, you are compromised by using only an FPGA for processing and I / O connectivity in your system. FPGAs do not have the pilot ecosystem and the code / IP base that architectures and microprocessor operating systems do. In addition, microprocessors coupled with operating systems provide the basis for file structures and communication to devices used for many, often essential, tasks, such as saving data to disk.

As a result, over the last decade, hybrid architecture, sometimes referred to as a heterogeneous architecture, has emerged in which a microprocessor is paired with an FPGA that is then linked to I / O. This technique takes benefit of the benefits that these two goals offer. In recent years, companies such as Xilinx, with its family of Zynq targets, have adopted this approach and published solutions that combine the processor and FPGA on a single chip to create this hybrid architecture.
V. CONCLUSION

This paper presents a brief review of various inverter techniques. Here main objective of this review paper is to focus on multilevel inverters. We conclude various multilevel inverter techniques also review previously done work. In this also discuss the result parameters of VLSI.

REFERENCES


